APPLICATION UNDER UNITED STATES PATENT LAWS

Atty. Dkt. No. 040008-0307316

Invention: STI STRUCTURE AND FABRICATING METHODS THEREOF

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- ☐ Provisional Application
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- ☐ Continuing Application
  - ☐ The contents of the parent are incorporated by reference
- ☐ PCT National Phase Application
- ☐ Design Application
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SPECIFICATION

STI STRUCTURE AND FABRICATING METHODS THEREOF

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application relates to and claims priority to Korean Patent Application No. 10-2002-0039555, filed on June 18, 2003, which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a shallow trench isolation ("STI") structure and fabricating methods for the same. In particular, the present invention relates to an STI structure that can improve an operating speed of a transistor and a latch-up characteristic by changing the STI structure and fabricating methods thereof.

Description of Related Art

[0003] Figs. 1a-1e illustrate the process steps according a conventional STI fabricating method. In this conventional method, a pad oxide layer 2 is grown on a silicon substrate 1. A nitride layer 3 is then deposited on the pad oxide layer 2 as shown in Fig. 1a. The nitride layer 3, the pad oxide layer 2, and the silicon substrate 1 are then etched to form the trench, as shown in Fig. 1b. A thermal oxide layer 5 is then grown on the etched surface etched, as shown in Fig. 1c. An oxide layer 6 is then deposited on the thermal oxide layer 5 and the nitride layer 3 by atmospheric pressure chemical vapor deposition ("APCVD"). A densification process is then performed. Next, referring to Fig. 1d and Fig. 1e, chemical mechanical polishing ("CMP") is then performed, and, finally, the nitride layer 3 is removed using an HF wet etch to complete an STI forming process. Subsequently, a MOS transistor is then fabricated.

[0004] The MOS transistor fabricated by the above-described process may have a parasitic source/drain junction capacitor due to structural features of the structure. As a result, the operating speed of a transistor slows due to an increase in the gate RC delay. Furthermore, a junction between the bottom of source/drain and P-well or N-well may form, which can cause an IC chip to consume a large amount of electric power due to increased junction leakage.

[0005] Korean Patent Publication No. 10-1999-0061132 discloses a method for ensuring a process margin by insulating between cells using a silicon on insulator ("SOI") structure and a

STI structure to apply a back bias. The method includes performing an oxygen ion implantation for a P-type semiconductor substrate so that the oxygen ion is positioned on a desired depth. A trench is formed on the substrate with a SOI structure having a buried oxide layer formed by a thermal oxidation process and a silicon layer. An STI structure is formed to insulate between a cell in the P-type semiconductor substrate and a cell in the silicon layer so as to apply back bias This process, however, has settled a problem that the insulated layer is floated on the top of the buried oxide.

[0006] Figs. 2a-2e illustrate the process steps according to the fabricating method described in the above-mentioned Korean patent publication. A buried oxide layer 11 and a silicon layer 12 are formed on a semiconductor substrate 10, as shown in Fig. 2a. A trench 13 for making an STI is then formed by etching the silicon layer 12 and the buried oxide layer 11, as shown in Fig. 2b. A spacer 14 is then formed on the inside walls of the trench 13, as shown in Fig. 2c. A field-stop impurity area 15 is then formed in the substrate 10 under the trench 13, as shown in Fig. 2d. An insulating layer 16 is then formed to fill the trench, as shown in Fig. 2e.

[0007] This process forms a silicon layer 12 instead of a nitride layer on the buried oxide layer, and provides no clear means for forming the spacer 14. In addition, the spacer 14 is buried by the insulating layer 16, thereby increasing the probability of void formation. As such, this process cannot substantially reduce the source/drain junction capacitance and junction leakage. Furthermore, it cannot improve the operating speed of the transistor and the latch-up characteristic.

BRIEF SUMMARY OF THE INVENTION

[0008] Embodiments of the present invention are directed to an STI structure and fabricating methods thereof that substantially obviate one or more of the problems associated with limitations and disadvantages of the related art. An aspect of embodiments of the present invention is to provide a method for fabricating an STI that can improve the operating speed of the transistor and a latch-up characteristic by reducing source/drain junction capacitance and junction leakage. This can be achieved through a change of the STI structure. In accordance with embodiments of the present invention, a method for fabricating an STI is disclosed. The method includes forming a pad oxide layer and a first nitride layer on a substrate. A trench is then formed by etching the first nitride layer, the pad oxide layer and the substrate. The substrate is etched such that the trench is formed with an adequate depth. The substrate can be etched to a depth of approximately 2000Å. An oxide layer and a second nitride layer are then

deposited on the surface and the first nitride layer and in the trench. A spacer is then formed on the lateral walls of the trench by etching the second nitride layer. A buried oxide is grown in the substrate underneath the trench by performing a thermal oxidation process on the substrate. The spacer is then removed. The trench is then filled by depositing an insulating layer. Finally, a planarization process is performed.

[0009] The STI fabricating method can substantially reduce a total parasitic capacitance. Therefore, gate RC delay is reduced and the operating speed of a transistor increases. In addition, the STI fabricating method can substantially reduce junction leakage because the junction between the bottom of the source/drain and N-well or P-well is not formed. The STI fabricating method can improve isolation characteristics of P-well and N-well, and increase a circuit design margin due to the improvement of latch-up characteristic.

[0010] In accordance with embodiments of the present invention, an STI structure is disclosed. The STI structure includes a trench formed on an isolation area of a substrate. An oxide layer is formed on the lateral walls of the trench. An insulating layer formed in the trench. The structure includes a buried oxide formed in the substrate underneath the trench. The buried oxide has a larger width than that of the trench.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention, wherein like reference numerals designate the elements:

[0012] Figs. 1a-1e illustrate, in cross-sectional views, the process steps according to a conventional STI fabricating method;

[0013] Figs. 2a-2e illustrate, in cross-sectional views, the process steps according to another conventional STI fabricating method; and

[0014] Figs. 3a-3i illustrate, in cross-sectional views, the process steps for fabricating STI according to a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0016] A pad oxide layer 22 is grown on a silicon substrate 21. A first nitride layer 23 is deposited on the pad oxide layer 22, as shown in Fig. 3a. A trench 24 is formed by patterning and etching the first nitride layer 23, the pad oxide layer 22, and the substrate 21, as shown in Fig. 3b. The substrate 21 is etched to a depth of source/drain. The depth is preferably 2000Å. It is contemplated that the depth can be greater or less than 2000Å.

[0017] As shown in Fig. 3c, a tetraethyl orthosilicate ("TEOS") layer 25 is then deposited on the substrate 21. The TEOS layer 25 can preferably have a thickness between 225Å and 325Å. The TEOS layer 25 can be deposited by low pressure chemical vapor deposition ("LPCVD"). A second nitride layer 26 is deposited on the TEOS layer 25 by LPCVD. The second nitride layer 26 can preferably have a thickness between 250Å and 350Å instead of depositing the TEOS layer by LPCVD, a thermal oxide may be grown on the exposed silicon substrate. The TEOS layer 25 can be deposited on the thermal oxide by LPCVD.

[0018] A nitride spacer 27 is formed by removing all of the nitride layer 26 except for the nitride on the lateral walls of the trench 24, as shown in Fig. 3d. This can be performed by blanket etching. The nitride spacer 27 prevents oxygen from penetrating into the lateral walls of the trench 2 and reacting with the silicon substrate 21 during a wet oxidation process. The substrate 21 is exposed in the bottom of the trench 24, as shown in Fig. 3d.

[0019] The exposed silicon substrate 21 is oxidized by a wet oxidation process. The oxidation of the silicon substrate 21 is performed horizontally, as well as, vertically. The oxide is not formed on the lateral walls of the trench 24 because the nitride spacer 27 prevents the penetration of oxygen. Instead, an oval-type buried oxide 28 is grown, as shown in Fig. 3e. The buried oxide 28 is preferably thicker than the P-well or N-well. The buried oxide 28 has an adequate width so that the buried oxide is not in contact with another adjacent buried oxide, as shown in Fig. 3e. The nitride spacer 27 can then be removed using an HF wet etch, as shown in Fig. 3f. An oxide 29 is deposited to fill the trench 24. The oxide 29 can be deposited by APCVD. Then, a densification process and a CMP process are performed in sequence. As shown in Fig. 3h, the remaining first nitride layer 23 is removed. The nitride layer 23 can be removed using phosphoric acid to form the STI structure.

[0020] Subsequently, an adequate impurity is implanted into an active area by ion implantation, as illustrated in Fig. 3i. Here, the pad oxide layer 22 on the active area is used as a screening oxide. A gate insulation layer 30 is then grown and a polysilicon layer is deposited thereon. The gate insulation layer and the polysilicon layer are patterned and etched to form a gate 31. An LDD region 32 is then formed by ion implantation. A sidewall spacer 35 is formed

on the lateral walls of the gate 31 by depositing a sidewall nitride layer and performing a blanket etch. A source/drain region 33 is formed by ion implantation. The source/drain region 33 is in contact with the buried oxide 18.

[0021] A silicide layer 34 is formed by a silicide process. Then, a pre-metal dielectric liner layer and pre-metal dielectric boron-phosphorus silicate glass ("PMDBPSG") layer 36 are deposited in turn, and planarized by CMP. A capping oxide is deposited on the PMD BPSG layer 36. At least one contact hole 37 is formed through a contact patterning/etching process. The contact hole 37 is filled with tungsten and flattened by CMP. Finally, through a metal process a source/drain electrode, a gate electrode and a body electrode collectively identified 38 are formed.

[0022] An STI fabricating method according to embodiments of the present invention can prevent formation of a parasitic source/drain junction capacitor because the bottom of the source/drain is in contact with the buried oxide, which substantially reduces total parasitic capacitance Furthermore, gate RC delay is reduced and the operating speed of the transistor increased. The STI fabricating method in accordance with embodiments of the present invention can substantially reduce junction leakage because the junction between the bottom of the source/drain and N-well or P-well is not formed, which reduces the consumption of electric power by an IC chip because a leakage current decreases.

[0023] The STI fabricating method can improve isolation characteristics of the P-well and the N-well because a junction between the P-well and the N-well is not formed because the buried oxide 28 is thicker than the P-well or the N-well, and can increase a circuit design margin due to the improvement of the latch-up characteristic.

[0024] The foregoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The present teachings can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.